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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/741,857 | 12/22/2000 | Richard P. Modelski | P 270188 NOR-13180BA | 8573 |

34845 7590 11/13/2006

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| EXAMINER | |
|---|---|
| TRUONG, LAN DAI T | |
| ART UNIT | PAPER NUMBER |
| 2152 | |

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/741,857 | MODELSKI ET AL. | |
| | Examiner | Art Unit | |
| | Lan-Dai Thi Truong | 2152 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09/052006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3; 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3; 5-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/05/2006 has been entered.

2. This action is response to communications: application, filed on 12/22/2000; amendment filed 09/05/2006. Claims 1-3, 5-18 are pending; claim 4 is cancelled; claims 1-3, 5, 17 are amended

3. The applicant's arguments filed on 09/05/2006 have fully considered but they are moot in view with new ground for rejections

## Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or descried as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 1, 5, 17 are rejected under 35 U.S.C 103(a) as being un-patentable over Berenbaum et al. (U.S. 7,096,343) in view of Davis et al. (U.S. 5,357,617)**

***Regarding to claim 1:***

Berenbaum discloses the invention substantially as claimed, including a method, which can be implemented in a computer hardware or software code for processing a plurality of independent multi-packet threads comprising:

Retrieving a first packet from a first multi-packet thread: Bernbaum discloses method for including instruction packet for each thread of multi-threads system. Bernbaum also discloses method for fetching instruction packets in threads, and sending them to execution pipeline stages: (column 3, lines 1-67; column 4, lines 6-7; column 5, lines 20-67; column 6, lines 5-17, lines; column 7, lines 57-67)

Retrieving a second packet from a second multi-packet thread: as similar as rejection provided for limitation above, Bernbaum discloses method for fetching instruction packets in threads: (column 3, lines 1-67; column 4, lines 6-7; column 5, lines 20-67; column 6, lines 5-17, lines; column 7, lines 57-67)

However, Bernbaum does not explicitly disclose processing the first packet in a first stage of a processing pipeline; forwarding the first packet to a next stage of the processing while forwarding the second packet to the first stage of the processing pipeline such that the first packet and the second packet can be executed simultaneously in the processing pipeline

In analogous art, Davis discloses a hybrid pipelined processor which handles substantially concurrent instruction threads; wherein a hybrid pipelined processor includes multiple states as fetch stage, decode stage and execution stage. Each of instruction thread moves

subsequently from a first stageto the next stage and then keeps going. While one instruction thread moves to a next stage from a first stage, the other instruction thread moves into the first state: (column 2, lines 47-67)

The independence of the multi-packet-threads eliminates packet processing delay: Davis discloses one of advantages of using multithreads system is elimination the delay of processing time: (column 2, lines 1-9; column 8, lines 15-20)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Davis's ideas of moving instruction thread subsequently from a first stage to a next stage and then keeps going. While one instruction thread moves to a next stage from a first stage, the other instruction thread moves into the first stage with Bernbaum's system in order to reduce delay of processing time, see (column 8, lines 10-20)

***Regarding to claim 5:***

This claim is rejected under rationale of claim 1

***Regarding to claim 17:***

In addition to rejection in claim 5, Bernbaum Davis further discloses each multi-packet thread is a thread identifier identifying a subset registers allocated to corresponding independent multi-packet threads, the subset of registers selected from among a set of registers, and wherein the subsets associated with each one of the plurality of independent multi-packet threads are unique: Davis discloses multiple independent instruction threads register to multiple-threads processor: (abstract, lines 4-9; column 5, lines 32-67; column 6, lines 1-60)

**Claims 2-3 are rejected under 35 U.S.C 103(a) as being un-patentable over Bernbaum-Davis in view of Epps et al. (U.S. 6,813,243)**

***Regarding to claim 2:***

Bernbaum-Davis discloses the invention substantially as disclosed in claim 1, but does not explicitly teach transferring packet from an input buffer to a packet task manager; dispatching the packet from the packet task manager to an analysis machine; classifying the packet in the analysis machine; and modifying and forwarding the packet in a packet manipulator

However, Epps teaches methods for transferring data from an input buffer (Fig 2, item 215) to a packet task manager (Fig 2, item 130, Col. 5, lines 50-55); dispatching the data from the packet task manager to an analysis machine (Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); classifying the data in the analysis machine (Col. 6, lines 33-37); and modifying and forwarding the data in a packet manipulator (Fig 4, item 450 and 460; Col. 6, lines); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of incorporating processes of transferring data to a packet task manager; dispatching the data from the packet task manager to an analysis machine; classifying the data in the analysis machine; modifying and forwarding the data in a packet manipulator with Bernbaum-Davis's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

***Regarding to claim 3:***

Bernbaum-Davis discloses the invention substantially as disclosed in claim 1, but does not explicitly teach forwarding data to output after modifying

However, Epps teaches forwarding packet to output after modifying (Epps, Fig. 2, item 1430; Col. 42, lines 10-21)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of modifying and forwarding the data in a packet manipulator with Bernbaum-Davis's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

**Claims 6-16 and 18 are rejected under 35 U.S.C 103(a) as being un-patentable over Bernbaum-Davis in view of Epps et al. (U.S. 6,813,243) and further in view of Eickemeyer (U.S. 6,694,425)**

***Regarding to claim 6:***

Bernbaum-Davis discloses the invention substantially as disclosed in claim 5, but does not explicitly teach wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field (Epps, Col. 6, lines 50-67; Col. 14, lines 1-3); a packet task manager (Epps, Fig 2, item 130, Col. 5, lines 50-55) operationally connected to said analysis machine (Epps, Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460).

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Epps's ideas of co-operating processes of packet task manager; dispatching the data from the packet task manager to an analysis machine; classifying the data in the analysis machine; modifying and forwarding the data in a packet manipulator with

Bernbaum-Davis's system in order to improve the communication rates, see (Epps, Col. 3, lines 39-45)

However, Bernbaum-Davis- Epps does not explicitly disclose a machine having multiple pipelines

In analogous art, Eickemeyer discloses the decode unit may have multiple pipelines: (column 9, lines 19-24)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Eickemeyer's ideas including multiple pipelines in a system with Bernbaum-Davis- Epps's system in order to provide a flexible multithreads communication system, see (Eickemeyer: column 9, lines 18-41)

***Regarding to claim 7:***

In addition to rejection in claim 6, Bernbaum -Davis- Epps-Eickemeyer further discloses multi-threaded analysis machine: Bernbaum discloses a multi-threads system includes an "allocation mechanism" which is equivalent to "multi-threaded analysis machine": (column 5, lines 1-30; column 6, lines 5-17, lines; column 7, lines 57-67)

***Regarding to claim 8:***

In addition to rejection in claim 6, Bernbaum -Davis- Epps Eickemeyer further discloses that analysis machine has 32 threads, although Bernbaum -Davis- Epps Eickemeyer does not specifically disclose analysis machine has 32 threads, such limitations are merely a matter of design choice and would have been obvious in system of Bernbaum -Davis- Epps Eickemeyer

***Regarding to claim 9:***

In addition to rejection in claim 6, Bernbaum -Davis- Epps-Eickemeyer further discloses a packet task manager (Epps, Fig 2, item 130, Col. 5, lines 50-55) operationally connected to said analysis machine (Epps, Fig 2, data travel from item 215 to 220; Col. 6, lines 33-37); a packet manipulator (Epps, Fig 4, item 450, 460) operationally connected to said analysis machine (Epps, Fig 4, data travel from 220 to item 450 and 460); a global access bus including a master request bus (Epps, Fig 4, item 496) and a slave request bus (Epps, Fig 4, item 497) separated from each other and pipelined (Epps, Fig 4, items 410-460)

***Regarding to claim 10:***

In addition to rejection in claim 6, Bernbaum -Davis- Epps-Eickemeyer further discloses an external memory engine (Fig 4, item 215, external FIFO externally connected to analysis machine) operationally connected to said analysis machine (Epps, Fig 4, item 420, Col. 6, lines 30-35, wherein the analysis machine classifies packet data); a hash engine (Epps, Fig. 4, item 430; Col. 24, lines 24-28) operationally connected to said analysis machine (Epps, Col. 24, lines 24-28)

***Regarding to claims 11-12:***

In addition to rejection in claim 9, Bernbaum-Davis- Epps-Eickemeyer further discloses packet input global access bus program code (Epps: Col. 11, lines 55-60, wherein the instructions are the software code, Fig 6, item 610, 630) used for flow of data packet information from a flexible input data buffer (Epps, Fig 6, item 480) to an analysis machine (Epps, Fig 6, item 420; Col. 11, lines 55-60; Col. 6, lines 23-37, the packet header information is retrieved and processed by the pre-process stage)

***Regarding to claim 13:***

In addition to rejection in claim 9, Bernbaum-Davis- Epps-Eickemeyer further discloses statistics data global access bus software code (Epps: instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates theexecution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the packet manipulator) used for connection of an analysis machine (Fig 4, item 420) to a packet manipulator (Epps, Fig 4, item 460)

***Regarding to claim 14:***

In addition to rejection in claim 9, Bernbaum-Davis- Epps-Eickemeyer further discloses private data global access bus software code (Epps discloses instructions residing in pipeline control Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) for connection of an analysis machine (Fig 4, item 420) to an internal memory engine sub-module (Epps, Fig 4, item 480, Col. 11, lines 55-65, wherein the instruction fetches allows for connection between the PreP stage / analysis machine and the packet header buffer/ internal memory engine sub-module, look up is done through pipeline control Fig 4, item 495)

***Regarding to claim 15:***

In addition to rejection in claim 9, Bernbaum-Davis- Epps-Eickemeyer further discloses lookup global access bus software code (Epps discloses instructions residing in pipeline control

Fig 4, item 495; Col. 11, lines 55-65, wherein instructions originated from pipeline control 495 dictates the execution of the stages note, that the packet data is passed to the next stage upon completion of the current stage of execution, therefore, pipeline control is used for communications purposes between analysis machine and the internal memory engine) used for connection of an analysis machine (Fig 4, item 420) to an internal memory engine sub-module (Epps, Fig 4, item 480, Col. 11, lines 55-65, wherein the instruction fetches allows for connection between the PreP stage / analysis machine and the packet header buffer/ internal memory engine sub-module, look up is done through pipeline control Fig 4, item 495)

***Regarding to claim 16:***

In addition to rejection in claim 9, Bernbaum-Davis- Epps-Eickemeyer further discloses results global access bus software code (Epps, Col. 10, lines 5-10, the value of n is a programmable value, indicating amount of data to send to fetch stage, Fig 5, item 410) used for providing flexible access to an external memory (Epps, Col. 10, lines 5-10, amount of data received can be adjusted)

***Regarding to claim 18:***

In addition to rejection in claim 9, Bernbaum-Davis- Epps-Eickemeyer further discloses a bi-directional access port operationally connected to said analysis machine (Epps, Col. 25, lines 1-7, wherein the input/output port are PPP/HDLC); an input buffer (Epps, Fig 2, item 215) operationally connected to said analysis machine (input buffer operationally connected to Prep Stage Fig 4, item 420 / analysis machine through the pipeline); and an output buffer (Epps, Fig 2, item 1430) operationally connected to said analysis machine (transmit FIFO operationally connected to Prep Stage Fig. 4, item 420 through the switch fabric)

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "Multi-thread packet processor": 7093109; 6952824; 5764912; 6976095; 6768716

**Conclusions**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan-Dai Thi Truong whose telephone number is 571-272-7959. The examiner can normally be reached on Monday- Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob A. Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

11/06/2006

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